Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (*Currently Amended*) In an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;

forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;

forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;

~~coupling together said first and second metal interconnect structures at a top metal layer prior to programming;~~

forming a one cycle ladder structure, using the first and second metal interconnect structures, that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer;

coupling one of the first and second supply potentials to at least one of said first and second metal interconnect structures to form an output; and

altering at least one of the plurality of metal layers to thereby program the output.

2. (*Original*) The method of claim 1, further comprising forming multiples of the first and second metal interconnect structures and coupling together the first and second metal interconnect structures to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

3. (*Canceled*).

4. (*Currently Amended*) The method of claim [[3]] 1, further comprising forming the ladder structure in a shape of a cube.

5. (*Currently Amended*) The method of claim 4, further comprising forming the first and second supply potentials as two buses located in a central region of said cube-shaped structure [[and]] so as to be accessible at each of the metal layers.

6. (*Currently Amended*) The method of claim [[4]] 1, further comprising forming the ladder structure in a shape of a spiral.

7. (*Original*) The method of claim 6, further comprising forming the first and second supply potentials as buses accessible at each of the metal layers.

8. (*Original*) The method of claim 1, further comprising altering any one of the plurality of metal layers to thereby reprogram at least one of the first and second metal interconnect structures.

9. (*Original*) The method of claim 8, further comprising repeating the reprogramming.

10. (*Original*) The method of claim 1, further comprising altering any one of a plurality of via layers to thereby reprogram at least one of first and second metal interconnect structures.

11. (*Original*) The method of claim 10, further comprising repeating the reprogramming.

12. (*Original*) The method of claim 1, further comprising altering any one of the plurality of metal layers or any one of a plurality of via layers to thereby reprogram the first and second metal interconnect structures.

13. (*Original*) The method of claim 12, further comprising repeating the reprogramming.

14-27. (*Canceled*).

28. (*Currently Amended*) In an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;

forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;

forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;

~~coupling together said first and second metal interconnect structures at a top metal layer prior to programming;~~

forming a one cycle ladder structure in the shape of a cube using multiples of the first and second metal interconnect structure that traverse the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer;

coupling the first supply potential to the first interconnect structure and the [[and]] second supply potential to the second interconnect structure to form at least one output; and

altering at least one of the plurality of metal layers to thereby program at least one of the outputs.

29. (*New*) The method of claim 28, further comprising forming the first and second supply potentials as two buses located in a central region of said cube-shaped structure so as to be accessible at each of the metal layers.

30. (*New*) In an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;

forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;

forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;

forming a one cycle ladder structure in the shape of a spiral that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer;

coupling the first supply potential to the first interconnect structure and the second supply potential to the second interconnect structure to form at least one output; and

altering at least one of the plurality of metal layers to thereby program at least one of the outputs.

31. (*New*) The method of claim 30, further comprising forming the first and second supply potentials as buses accessible at each of the metal layers.